What is claimed is:

1. A mode entrance control circuit of a semiconductor memory device, comprising:

an operation control part for generating an operation enable signal when a first voltage applied through a first pad is over a first determination voltage;

a voltage division part for dividing a second voltage applied through a second pad to generate a trimming reference voltage; and

a mode entrance signal generating part that operates in response to the operation enable signal, for comparing a level of an applied fixed reference voltage with a level of the trimming reference voltage and for generating a mode entrance enable signal that allows the semiconductor memory device to enter into a predetermined mode.

2. The control circuit as claimed in claim 1, wherein a level of the first and second voltages is higher than that of an operation voltage source of the semiconductor memory device.

3. The control circuit as claimed in claim 2, wherein the level of the second voltage is higher than the level of the first voltage.

4. The control circuit as claimed in claim 2, wherein the level of the second voltage is equal to the level of the first voltage.

5. The control circuit as claimed in claim 3, wherein the mode entrance signal generating part comprises a differential amplifier of a current mirror type for amplifying a difference between the level of the fixed reference voltage and the level of the trimming reference voltage in response to the operation enable signal.

6. The control circuit as claimed in claim 5, wherein the operation control part comprises:

a PMOS transistor and a plurality of NMOS transistors having source-drain or drain-source channels connected in series between the first pad and a ground; and

an inverter connected to the drain of the PMOS transistor, and an output inverter for inverting an output of the inverter.

7. The control circuit as claimed in claim 6, wherein the voltage division part comprises:

a plurality of PMOS and NMOS transistors having source-drain or drain-source channels connected in series between the second pad and the ground; and

upper fuses and lower fuses which can be cut by a light source.

8. The control circuit as claimed in claim 3, wherein the mode entrance signal generating part is constructed of a differential amplifier of a current mirror type, wherein the differential amplifier comprises:

PMOS transistors having sources that receive in common the operation voltage source and having gates that are connected with each other;

NMOS transistors having drains that are respectively connected with drains of the PMOS transistors; and

an NMOS transistor having a drain that is coupled with a common source of the NMOS transistors, a source that is grounded, and a gate that receives the operation enable signal.

9. The control circuit as claimed in claim 7, wherein a mode entrance is allowed only when a voltage higher than a previous voltage is applied when a cutting number of the upper fuses is increased.

10. A method of generating a mode entrance control signal in a semiconductor memory device, comprising:

preparing a trimming reference voltage determination part composed of a plurality of MOS transistors and fuses;

determining a trimming reference voltage by cutting the fuses;

applying a first voltage over a first determination voltage through a first pad, and generating an operation enable signal;

applying a second voltage through a second pad, and generating the trimming reference voltage; and

comparing a level of an applied fixed reference voltage with a level of the trimming reference voltage during the generation of the operation enable

signal, and generating a mode entrance enable signal to allow the semiconductor memory device to enter into a predetermined mode.

11. The method as claimed in claim 10, wherein the first and second voltages have a level higher than that of an operation voltage source of the semiconductor memory device.

12. The method as claimed in claim 11, wherein the level of the second voltage is higher than the level of the first voltage.

13. The method as claimed in claim 11, wherein the level of the second voltage is equal to the level of the first level.

14. The method as claimed in claim 11, wherein the fixed reference voltage is a reference voltage generated from a reference voltage generator of the semiconductor memory device.